LOCALIZED OXIDE TRAPPED CHARGE'S EFFECT ON THE CAPACITANCE BETWEEN GATE-SOURCE IN FINFET DEVICES

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Abstract. This study examines the effect of localized oxide trapped charge on the capacitance of the gate-to-source (drain) connection in silicon-on-insulator (SOI) based FinFET devices. The capacitance-voltage characteristics of the gate-source capacitance are analyzed using a small AC signal technique. The gate-source (gate-drain) capacitance is evaluated at various positions along the channel where the localized oxide trapped charge is present. Additionally, the distribution of charge carriers along the channel at different locations of the localized oxide trapped charge is taken into account. The results demonstrate a consistent increase in the gate-source capacitance as the distance between the source-channel boundary and the center of the localized charge increases.

Keywords: Capacitance-Voltage (C-V) characteristics, oxide trapped charge, silicon-on-Insulator (SOI), doping level, depletion layer, charge distribution.

Introduction. MOSFETs, particularly FinFETs, can experience degradation due to electrical stress or radiation, impacting their performance. Key degradation mechanisms include hot carrier injection, bias temperature instability, off stress, and radiation-induced charge accumulation. These effects result from charges trapped in the oxide layer or at the interface, necessitating careful consideration in the design of analog and digital integrated circuits. Charge trapping in the oxide affects MOSFET parameters such as threshold voltage, subthreshold slope, and transconductance, which lead to performance degradation. To analyze charge trapping mechanisms, it is essential to develop methods for estimating the localization and distribution of trapped charge along the channel. A practical diagnostic approach involves measuring the capacitance-voltage characteristics of lateral source (drain)-channel p-n junctions, as experimentally validated in the literature. Non-uniform charge distribution in the oxide or at the semiconductor-oxide interface is reflected in these junctions, providing insights into charge trapping along the channel.

This study adapts this method, originally designed for planar MOSFETs, to SOI FinFETs. It focuses on the influence of oxide and interface-trapped charge on the capacitances of lateral source-channel (drain-channel) p-n junctions. In SOI FinFETs, the gate-source (or gate-drain) connection includes this capacitance (Cp-n), which

significantly contributes to the overall capacitance of the selected connection. The gate-source and gate-drain connections consist of gate oxide capacitance (Cox), depletion layer capacitance (Cdep), and source-channel p-n junction capacitance (Cp-n). In the proposed approach, only the barrier capacitance of the source-channel p-n junction is considered. A positive voltage is applied to the n-type source contact relative to the gate, inducing accumulation near the oxide-semiconductor interface, thereby excluding Cdep. Under these conditions, the resulting capacitance Cgs can be expressed as follows:

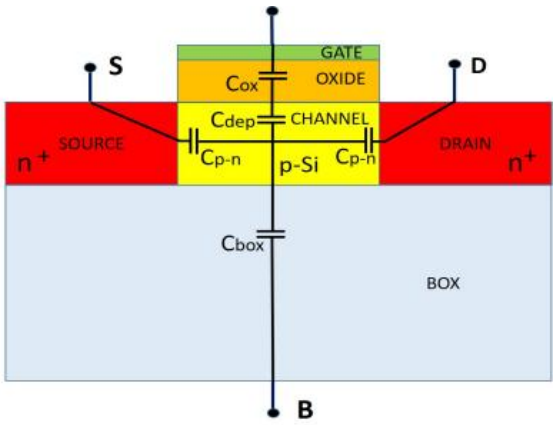
$$C_{gs} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{p-n}} \right)^{-1}$$

where Cox is the gate oxide capacitance per unit area, which remains independent of the applied voltage. Estimations indicate that the depletion layer width of the source-channel (drain-channel) p-n junction is approximately 0.1 μ, while the gate oxide thickness tox is 2.5 nm. Consequently, Cp−n is significantly smaller than Cox, leading to:

$$C_{gs} \approx C_{p-n}$$

Since Cp−n is highly sensitive to the distribution of trapped charge in the oxide, this study simulates the dependence of Cgs on the position of localized oxide-trapped charge along the channel.

Simulation conditions and transistor parameters. 3D simulation was provided by using Advanced TCAD Sentaurus. The C-V dependence of the gate-source (gate-drain) connections was simulated on the basis of the small AC signal method. It is used a 1 MHz frequency in the method. The structure of the simulated SOI FinFET is shown in Fig. 2. Gate length L_{gate} and gate oxide thickness are 25 nm and 2.5 nm respectively. The thicknesses of the channel T_{Si} and back oxide T_{box} are 30 and 100 nm respectively. The width of the channel is 12 nm. The doping level of the p-Si channel is $1 \cdot 10^{15}$ cm^{-3}.



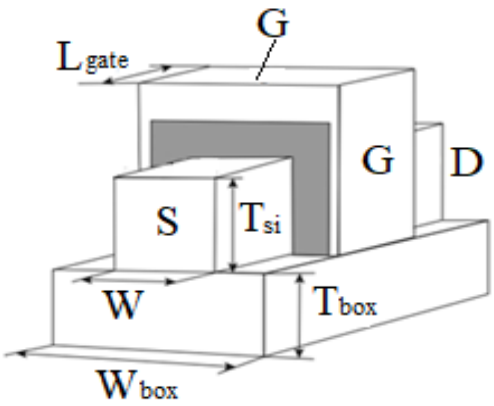


Fig.1. Cross-section of the simulated SOI FinFET with capacitances between contacts.

Fig.2. 3D structure of the simulated SOI FinFET

The capacitance C_{gs} of the gate-source connection is simulated at different distances between the center of the local oxide trapped charge and source-channel border. Local oxide trapped charge is modeled as a homogeneously charged area in the oxide layer. The density of charge in the charged area is 10^{12} cm^{-2} (or $4 \cdot 10^{18}$ cm^{-3}) and is appropriate to the value which can take place in MOSFET. Linear size of the local charge along channel d=5nm.

While the depletion layer width of the lateral source-channel (drain-channel) p-n-junction is more than the channel length, the local charge trapped in the oxide at a distance L from the border source-channel has impacts on the carrier distribution in the channel. Therefore this impact should be reflected in the capacitance of the source-channel junction and hence in the C-V dependence of the gate-source capacitance connection. FinFET has symmetry relative to the channel center and hence both capacitances of the gate-source and gate-drain connections should be the same. Therefore in the following, it is presented the results only for gate-source connection.

Simulation results and discussion. Results of the simulation of C-V dependence of the gate-source capacitance C_{gs} are shown in table 1. It is seen in the figure that at high applied voltages the capacitance C_{gs} significantly and monotonically depends on the position of the local trapped charge along the channel (Fig.3). Position L=2.5 nm is an exception in this dependence (Fig.3, point B) because in this position the local charge area is in contact with the end of the oxide layer.

C-V dependence of gate-source connection capacitance at different positions of the local trapped charge.

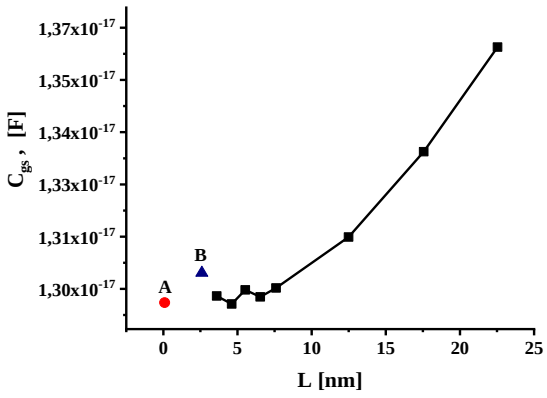


Fig.3. C_{gs} dependence on L at V_{gs}=4.5 V. Point A corresponds to the case when the local trapped charge is absent, point B corresponds to the

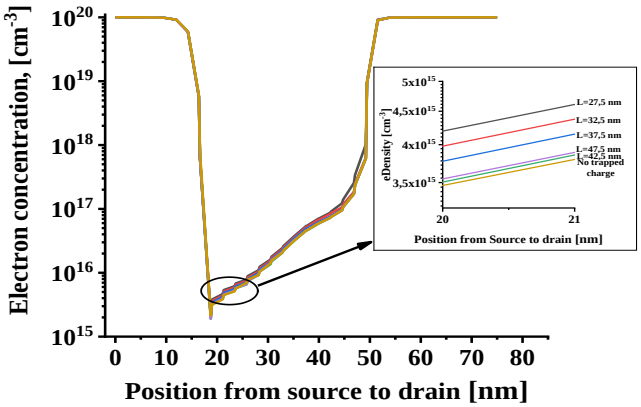


Fig4. Electron density distribution along the channel at depth 2nm from the channel surface, at different positions L of the local oxide trapped charge.

position of the local trapped charge at

L=2.5 nm.

The increase of the capacitance C_{gs} is connected with the influence of the local trapped charge on carrier concentration in the channel. The local charge trapped in the oxide layer increases the carrier concentration near the channel surface (fig.4) and as a result, the capacitance is increased. By definition capacitance is

$C_{gs} = dQ_V/dV$ (2)

here dQ_V is a change of the charge in the capacitor C_{gs} at a change the applied voltage by dV. At trapping the local charge in the gate oxide layer the electron concentration in the channel is changed and the charge in the C_{gs} capacitance is changed by dQ_{LC}. Therefore the formula (2) can be rewritten by the following expression

$C_{gs} = (dQ_V + dQ_{LC})/ dV$ (3)

This expression explains the increase of the capacitance C_{gs}.

At position L= 2.5 nm of the oxide trapped charge the configuration of the capacitance C_{gs} is changed because the local charge will be in contact with the end of the oxide layer (Fig.5). In this case the electron density in the channel surface will be redistributed which result in sufficiently increasing the capacitance C_{gs} more than in unbiased case and relatively capacitances corresponding to other positions (Tab.1). At high applied voltages the redistribution of the carrier densities leads to increasing the C_{gs} with increasing L (Fig.7).

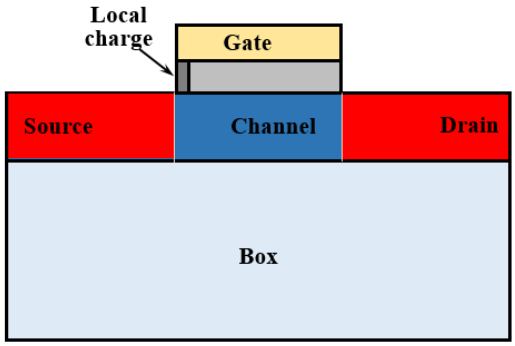


Fig.5. Cross-section of the FinFET with local charge trapped in oxide and which is located at the end of oxide layer. L=2.5 nm.

Due to the symmetry of the FinFET dependence of the gate-drain connection capacitance C_{gd} on the L should be reverse relative dependence C_{gs} on L, which means the decreasing C_{gd} with increasing L (Fig.7). C_{gs} and C_{gd} dependences on the L can be used for estimation the position of the local charge trapped in oxide along the channel. For this purpose, the ratio C_{gd}/C_{gs} dependence on L can be used (Tab.2).

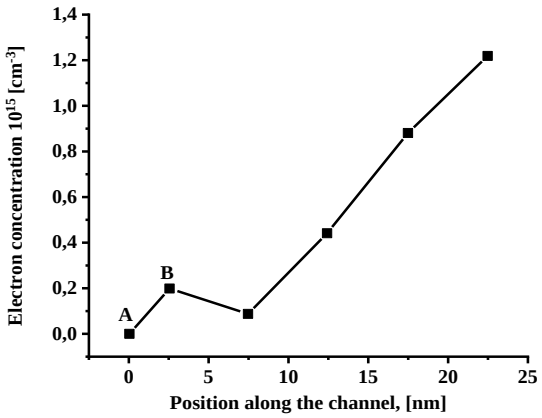


Fig.6. The change of the electron density in the channel at a depth 2 nm from the surface at trapping the local charge in the oxide layer at the different positions. A is point is the case without trapped charge, and B is the position with L=2.5 nm.

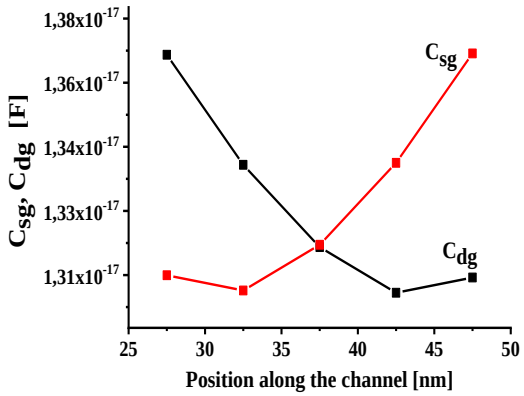


Fig.7. C_{gs} and C_{gd} dependence on the position of the local oxide trapped charge along the channel.

It is seen in the tab.2 that if the local charge trapped is trapped in the oxide in the source side from the channel center the ratio C_{gd}/C_{gs} is less than 1, and if the local charge is trapped in the drain side from the center of the channel the ratio is more than 1. If the local charge trapped in the center along the channel the ratio C_{gd}/C_{gs} is equal to 1.

The ratio C_{gs}/C_{gd} dependence on the position of the local oxide trapped charge along the channel.

Table. 1

	2,50E-09	0,95726
	7,50E-09	0,9751
	1,25E-08	1,00048
	1,75E-08	1,02642
	2,25E-08	1,04541

Conclusion. The simulation results indicate that in an SOI FinFET, at certain applied voltages, the gate-source capacitance exhibits a monotonic dependence on the location of the trapped charge within the oxide. This behavior is attributed to the impact of the localized charge on the distribution of carriers at the channel surface.

An exception to this dependence occurs when the trapped charge is positioned at the edge of the oxide layer. Additionally, it has been demonstrated that the ratio C_{gd}/C_{gs} varies linearly with the position of the trapped oxide charge along the channel

in an SOI FinFET. This relationship provides a basis for developing a method to verify charge trapping and estimate the spatial distribution of trapped charge within the channel.

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